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Date:		September 22, 2005
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From:	Name:	**Manu Kashyap, Intellectual Property Paralegal**
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	Re:	10/634,634
	Number of Pages Including this Page	19

MESSSAGE:

Docket Number: 03-0339
Box: IDS
Group Art: 2825
Examiner: Naum B. Levin

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(to be used for all correspondence after initial filing)

Application Number	10/634,634
Filing Date	August-04, 2003
First Named Inventor	Christopher Hamlin
Group Art Unit	2825
Examiner Name	Levin, Naum B.
Attorney Docket Number	03-0339
Total number of pages in this submission	18

ENCLOSURES *(check all that apply)*

- [ ] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Response
  - [ ] After Final
  - [ ] Affidavits(s)/declaration(s
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- [X] Information Disclosure Statemen
- [ ] Certified Copy of Priority Document(s)
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- [ ] Assignment Papers
- [ ] Drawing(s)
- [ ] Licensing-related Paper
- [ ] Petition Routing Slip (PTO/SB/69) and Accompanying Petition
- [ ] To Convert a Provisional Application
- [ ] Power of Attorney, Change of Correspondence Address
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1. Return address postcard for PTO mailroom to date stamp.

Remarks

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Individual Name	Timothy Croll, Reg. No. 36,771, Phone: [+1] 408-433-7475
Signature	T Croll
Date	22 Sept 05

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In re Application of :		§		
	Christopher Hamlin	§		
Serial No. :	10/634,634	§	**Group Art Unit :**	2825
Filed :	August 04, 2003	§	**Examiner :**	Levin, Naum B.
For :	Method and Apparatus for Mapping Platform-Based Design to Multiple Foundry Processes	§	**Atty Docket :**	/ 03-0339

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Dear Sir:

The references listed in the attached form, copies of which are attached, may be material to examination of above-identified application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR 1.56 and 1.97.

It is requested that the information disclosed herein be made of record in the application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

If it is determined that any additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 12-2252.

Respectfully submitted,

Timothy Croll

Reg. No. 36,771

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Date: 22 Sept 05

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Sheet 1 of 1

Complete if Known	
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Filing Date	August-04, 2003
First Named Inventor	Christopher Hamlin
Group Art Unit	2825
Examiner Name	Naum B. Levin
Attorney Docket No.	/ 03-0339

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, caalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where	T
		Mosis Scalable CMOS (SCMOS) design rules (Revision 8.0) updated 4/25/2003; http://www.mosis.org/technical/designrules/scmos/scmos-main.html; 4/30/03. Pgs 1-14	

Examiner signature		Date considered	

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MOSIS Scalable CMOS (SCMOS) Design Rules (Revision 8.0)

Updated: April 25, 2003

ABOUT MOSIS	PRODUCTS	CUSTOMER SERVICE	REFERENCE	HOME
NEWS	ORDERS	TECHNICAL SUPPORT	WEB FORMS	SITE MAP

MOSIS
4676 Admiralty Way
7th floor
Marina del Rey, CA 90292-6695

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1. Introduction

This document defines the official MOSIS scalable CMOS (SCMOS) layout rules. It supersedes all previous revisions.

MOSIS Scalable CMOS (SCMOS) is a set of logical layers together with their design rules, which provide a nearly process- and metric-independent interface to all CMOS fabrication processes available through MOSIS. The designer works in the abstract SCMOS layers and metric unit ("lambda"). He then specifies which process and feature size he wants the design to be fabricated in. MOSIS maps the SCMOS design onto that process, generating the true logical layers and absolute dimensions required by the process vendor. The designer can ofter submit exactly the same design, but to a different fabrication process or feature size. MOSIS alone handles the new mapping.

By contrast, using a specific vendor's layers and design rules ("vendor rules") will yield a design which is less likely to be directly portable to any other process or feature size. Vendor rules usually need more logical layers than the SCMOS rules, even though both fabricate onto exactly the same process. More layers means more design rules, a higher learning curve for that one process, more interactions to worry about, more complex design support required, and

longer layout development times. Porting the design to a new process will be burdensome.

SCMOS designers access process-specific features by using MOSIS-provided abstract layers which implement those features. For example, a designer wishing to use second-poly would use the MOSIS-provided second-poly abstract layer, but must then submit to a process providing for two polysilicon layers. In the same way, designers may access multiple metals, or different types of analog structures such as capacitors and resistors, without having to learn any new set of design rules for the more standard layers such as metal-1.

Vendor rules may be more appropriate when seeking maximal use of silicon area, more direct control over analog circuit parameters, or for very large production runs, where the added investment in development time and loss of design portability is clearly justified. However the advantages of using SCMOS rules may far outweigh such concerns, and should be considered.

1.1 SCMOS Design Rules

In the SCMOS rules, circuit geometries are specified in the Mead and Conway's lambda based methodology [1]. The unit of measurement, lambda, can easily be scaled to different fabrication processes as semiconductor technology advances.

Each design has a technology-code associated with the layout file. Each technology-code may have one or more associated options added for the purpose of specifying either (a) special features for the target process or (b) the presence of novel devices in the design. At the time of this revision, MOSIS is offering CMOS processes with feature sizes from 1.5 micron to 0.18 micron.

---

2. Standard SCMOS

The standard CMOS technology accessed by MOSIS is a single polysilicon, double metal, bulk CMOS process with enhancement-mode n-MOSFET and p-MOSFET devices [3].

2.1. Well Type

The Scalable CMOS (SC) rules support both *n*-well and *p*-well processes. MOSIS recognizes three base technology codes that let the designer specify the well type of the process selected. SCN specifies an *n*-well process, SCP specifies a *p*-well process, and SCE indicates that the designer is willing to utilize a process o either *n*-well or *p*-well.

An SCE design must provide both a drawn *n*-well and a drawn *p*-well; MOSIS wil use the well that corresponds to the selected process and ignore the other well. As a convenience, SCN and SCP designs may also include the other well (*p*-well in an SCN design or *n*-well in an SCP design), but it will always be ignored.

MOSIS currently offers only *n*-well processes or foundry-designated twin-well processes that from the design and process flow standpoints are equivalent to *n*-well processes. These twin-well processes may have options (deep *n*-well) that provide independently isolated *p*-wells. For all of these processes at this time use the technology code SCN. SCP is currently not supported, and SCE is treated exactly as SCN.

2.2. SCMOS Options

SCMOS options are used to designate projects that use additional layers beyond the standard single-poly, double metal CMOS. Each option is called out with a designator that is appended to the basic technology-code. Please note that not all possible combinations are available. The current list is shown in Table 1.

MOSIS has not issued SCMOS design rules for some vendor-supported options. For example, any designer using the SCMOS rules who wants the TSMC Thick_Top_Metal must draw the top metal with an eye upon the TSMC rules for that layer. Questions about other non-SCMOS layers should be directed to support@mosis.org.

Table 1: SCMOS Technology Options

Designation	Long Form	Description
E	Electrode	Adds a second polysilicon layer (poly2) that can serve either as the upper electrode of a poly capacitor or (1.5 micron only) as a gate for transistors
A	Analog	Adds electrode (as in E option), plus layers for vertical NPN transistor pbase
3M	3 Metal	Adds second via (via2) and third metal (metal3) layers

4M	4 Metal	Adds 3M plus third via (via3) and fourth metal (metal4) layers
5M	5 Metal	Adds 4M plus fourth via (via4) and fifth metal (metal5) layers
6M	6 Metal	Adds 5M plus fifth via (via5) and sixth metal (metal6) layers
LC	Linear Capacitor	Adds a cap_well layer for linear capacitors
PC	Poly Cap	Adds poly_cap, a different layer for linear capacitors
SUBM	Sub-Micron	Uses revised layout rules for better fit to sub-micron processes (see section 2.4)
DEEP	Deep	Uses revised layout rules for better fit to deep sub-micron processes (see section 2.4)

For options available to specific processes, see Tables 2a and 2b.

Table 2a: MOSIS SCMOS-Compatible Mappings

Foundry	Process	Lambda (micrometers)	Options
AMI	ABN (1.5 micron *n*-well)	0.80	SCNA, SCNE
AMI	C5N (0.5 micron *n*-well)	0.35	SCN3M, SCN3ME
Agilent/HP	AMOS14TB (0.5 micron *n*-well)	0.35	SCN3M, SCN3MLC
TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.25	SCN4ME
TSMC	0.35 micron 1P4M (4 Metal Silicided, 3.3 V/5 V)	0.25	SCN4M

Table 2b: MOSIS SCMOS_SUBM-Compatible Mappings

Foundry	Process	Lambda (micrometers)	Options

AMI	C5N (0.5 micron *n*-well)	0.30	SCN3M_SUBM, SCN3ME_SUBM
Agilent/HP	AMOS14TB (0.5 micron *n*-well)	0.30	SCN3M_SUBM, SCN3MLC_SUBM
TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.20	SCN4ME_SUBM
TSMC	0.35 micron 1P4M (4 Metal Silicided, 3.3 V/5 V)	0.20	SCN4M_SUBM
TSMC	0.25 micron 5 Metal 1 Poly (2.5 V/3.3 V)	0.15	SCN5M_SUBM
TSMC	0.18 micron 6 Metal 1 Poly (1.8 V/3.3 V)	0.10	SCN6M_SUBM

Table 2c: MOSIS SCMOS_DEEP-Compatible Mappings

Foundry	Process	Lambda (micrometers)	Options
TSMC	0.25 micron 5 Metal 1 Poly (2.5 V/3.3 V)	0.12	SCN5M_DEEP
TSMC	0.18 micron 6 Metal 1 Poly (1.8 V/3.3 V)	0.09	SCN6M_DEEP

2.3. SCMOS-Compatible Processes

MOSIS currently offers the fabrication processes shown above in Tables 2a, 2b, and 2c. For each process the list of appropriate SCMOS technology-codes is shown.

2.4. SCMOS_SUBM and SCMOS_DEEP Rules

The SCMOS layout rules were historically developed for 1.0 to 3.0 micron

processes. To take full advantage of sub-micron processes, the SCMOS rules were revised to create SCMOS_SUBM. By increasing the lambda size for some rules (those that didn't shrink as fast in practice as did the overall scheme of things), the sub-micron rules allow for use of a smaller value of lambda, and better fit to these small feature size processes.

The SCMOS_SUBM rules were revised again at the 0.25 micron regime to better fit the typical deep submicron processes, creating the SCMOS_DEEP variant.

Table 3a lists the differences between SCMOS and SCMOS sub-micron. Table 3b lists the differences between SCMOS sub-micron and SCMOS deep.

Table 3a: SCMOS and SCMOS Sub-micron Differences Differences

Rule	Description	SCMOS	SCMOS sub-micron
1.1, 17.1	Well width	10	12
1.2, 17.2	Well space (different potential)	9	18
2.3	Well overlap (space) to transistor	5	6
3.2	Poly space	2	3
5.3, 6.3	Contact space	2	3
5.5b	Contact to Poly space to Poly	4	5
7.2	Metal1 space	2	3
7.4	Minimum space (when metal line is wider than 10 lambda)	4	6
8.5	Via on flat	2	Unrestricted
11.1	Poly2 width	3	7
11.3	Poly2 overlap	2	5
11.5	Space to Poly2 contact	3	6
13.2	Poly2 contact space	2	3
15.1	Metal3 width (3 metal process only)	6	5
15.2	Metal3 space (3 metal process only)	4	3

15.4	Minimum space (when metal line is wider than 10 lambda) (3 metal process only)	8	6
17.3	Minimum spacing to external Active	5	6
17.4	Minimum overlap of Active	5	6

Table 3b: SCMOS Sub-micron and SCMOS Deep Differences

Rule	Description	SCMOS sub-micron	SCMOS DEEP
3.2	Poly space over field	3	3
3.2.a	Poly space over Active		4
3.3	Minimum gate extension of Active	2	2.5
3.4	Active extension beyond Poly	3	4
4.3	Select overlap of Contact	1	1.5
4.4	Select width and space (p+ to p+ or n+ to n+)	2	4
5.3, 6.3	Contact spacing	3	4
8.1	Via width	2	3
9.2	Metal2 space	3	4
9.4	Minimum space (when metal line is wider than 10 lambda)	6	8
14.1	Via2 width	2	3
15.2	Metal3 space	3	4
15.4	Minimum space (when metal line is wider than 10 lambda) (for 4+ metal processes)	6	8

21.1	Via3 width	2	3
22.2	Metal4 space (for 5+ metal processes)	3	4
22.4	Minimum space (when metal line is wider than 10 lambda)	6	8
25.1	Exact size	2 x 2	3 x 3
26.2	Metal5 space	3	4
26.3	Minimum overlap of Via4 (for 5 metal process only)	1	2
26.4	Via4 overlap	6	8
29.1	Exact size	3 x 3	4 x 4
30.3	Minimum overlap of Via5	1	2

3. CIF and GDS Layer Specification

A user design submitted to MOSIS using the SCMOS rules can be in either Calma GDSII format [2] or Caltech Intermediate Form (CIF version 2.0) [1]. The two are completely interchangable. Note that all submitted CIF and GDS files have already been scaled before submission, and are always in absolute metric units -- never in lambda units.

GDSII is a binary format, while CIF is a plain ASCII text. For detailed syntax and semantic specifications of GDS and CIF, refer to [2] and [1] respectively.

In GDS format, a design layer is specified as a number between 0 and 255. MOSIS SCMOS now reserves layer numbers 21 through 62, inclusive, for drawn layout. Layers 0 through 20 plus layers 63 and above can be used by designers for their own purposes and will be ignored by MOSIS.

Users should be aware that there is only one contact mask layer, although several separate layers were defined and are retained for backward compatibility. A complete list of SCMOS layers is shown in Table 4, along with a list by technology code in Table 5.

Table 4: SCMOS Layer Map

Layer	GDS	CIF	CIF Synonym	Rule Section	Notes

MOSIS SCMOS Layout Design Rules (8.0)

N_WELL	42	CWN		1	
P_WELL	41	CWP		1	SCPxx
CAP_WELL	59	CWC		17, 18	SCN3MLC
ACTIVE	43	CAA		2	
THICK_ACTIVE	60	CTA		24	SCN4M (TSMC only), SCN4ME, SCN5M, SCN6M
PBASE	58	CBA		16	SCNA
POLY_CAP1	28	CPC		23	SCNPC
POLY	46	CPG		3	
SILICIDE_BLOCK	29	CSB		20	SCN3M (Agilent/HP only), SCN3MLC, SCN4M (TSMC only), SCN5M, SCN6M
N_PLUS_SELECT	45	CSN		4	
P_PLUS_SELECT	44	CSP		4	
POLY2	56	CEL		11, 12, 13	SCNE, SCNA, SCN3ME, SCN4ME
HI_RES_IMPLANT	34	CHR		27	SCN3ME
CONTACT	25	CCC	CCG	5, 6, 13	
POLY_CONTACT	47	CCP		5	Can be replaced by CONTACT
ACTIVE_CONTACT	48	CCA		6	Can be replaced by CONTACT
POLY2_CONTACT	55	CCE		13	SCNE, SCNA, SCN3ME, SCN4ME Can be replaced by CONTACT.
METAL1	49	CM1	CMF	7	
VIA	50	CV1	CVA	8	
METAL2	51	CM2	CMS	9	
VIA2	61	CV2	CVS	14	SCN3M, SCN3ME, SCN3MLC, SCN4M, SCN4ME, SCN5M, SCN6M
					SCN3M, SCN3ME,

METAL3	62	CM3	CMT	15	SCN3MLC, SCN4M, SCN4ME, SCN5M, SCN6M
VIA3	30	CV3	CVT	21	SCN4M, SCN4ME, SCN5M, SCN6M
METAL4	31	CM4	CMQ	22	SCN4M, SCN4ME, SCN5M, SCN6M
CAP TOP METAL	35	CTM		28	SCN5M. SCN6M
VIA4	32	CV4	CVQ	25	SCN5M, SCN6M
METAL5	33	CM5	CMP	26	SCN5M, SCN6M
VIA5	36	CV5		29	SCN6M
METAL6	37	CM6		30	SCN6M
DEEP N WELL	38	CDNW		31	SCN5M, SCN6M
GLASS	52	COG		10	
PADS	26	XP			Non-fab layer used to highlight pads
Comments	--	CX			Comments

Table 5: Technology-code Map

Technology code with link to layer map	Layers
SCNE	N well, Active, N select, P select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass
SCNA	N well, Active, N select, P select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass
SCNPC	N well, Active, N select, P select, Poly cap, Poly, Contact, Metal1, Via, Metal2, Glass
SCN3M	N well, Active, N select, P select, Poly, Silicide block (Agilent/HP only), Hi Res Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass
SCN3ME	N well, Active, N select, P select, Poly, Poly2, Hi Res Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass
	N well, Cap well, Active, N select, P select, Poly,

SCN3MLC	Silicide block, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass
SCN4M	N_well, Active, Thick_Active (TSMC only), N_select, P_select, Poly, Contact, Metal1, Via, Metal2, Via2, Metal3, Via3, Metal4, Glass
SCN4ME	N_well, Active, Thick_Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Via2, Metal3, Via3, Metal4, Glass
SCN5M	N_well, Active, Thick_Active, N_select, P_select, Poly, Silicide block, Contact, Metal1, Via, Metal2, Via2, Metal3, Via3, Metal4, Cap_Top_Metal, Via4, Metal5, Deep_N_Well, Glass
SCN6M	N_well, Active, Thick_Active, N_select, P_select, Poly, Silicide block, Contact, Metal1, Via, Metal2, Via2, Metal3, Via3, Metal4, Via4, Metal5, Cap_Top_Metal, Via5, Metal6, Deep_N_Well, Glass

4. Minimum Density Rule

Many fine-featured processes utilize CMP (Chemical-Mechanical Polishing) to achieve planarity. Currently, for MOSIS, the Agilent/HP 0.50 micron, the AMI 0.50 micron, and all the 0.35 micron (and smaller) processes are in this category. Effective CMP requires that the variations in feature density on layer be restricted.

See the following for more details.

5. Process-Induced Damage Rules - (otherwise known as "Antenna Rules") General Requirements

The "Antenna Rules" deal with process induced gate oxide damage caused wher exposed polysilicon and metal structures, connected to a thin oxide transistor, collect charge from the processing environment (e.g., reactive ion etch) and develop potentials sufficiently large to cause Fowler Nordheim current to flow through the thin oxide. Given the known process charge fluence, a figure of exposed conductor area to transistor gate area ratio is determined which

guarantees Time Dependent Dielectric Breakdown (TDDB) reliability requirements for the fabricator. Failure to consider antenna rules in a design may lead to either reduced performance in transistors exposed to process induced damage, or may lead to total failure if the antenna rules are seriously violated.

See the following for more details.

---

6. Stack via support by process and technology codes

Not all processes nor technology codes support stacked vias.

Table 6: Stacked Vias

Technology code with link to layer map	Process	Stacked vias
SCNE	AMI 1.50 (ABN)	No
SCNA	AMI 1.50 (ABN)	No
SCNPC	AMI 0.80 (CWL)	No
SCN3M	Agilent/HP 0.50 (AMOS14TB)	No
	AMI 0.50 (C5N)	Yes
SCN3ME	AMI 0.50 (C5N)	Yes
SCN3MLC	Agilent/HP 0.50 (AMOS14TB)	No
SCN4M	Agilent/HP 0.35 (GMOS10QA), TSMC 0.35	Yes
SCN4ME	TSMC 0.35	Yes
SCN5M	TSMC 0.25	Yes
SCN6M	TSMC 0.18	Yes

---

7. Half-lambda grid submissions

MOSIS Scalable design rules require that layout is on a 1/2 lambda grid. Any other gridding information may change without warning. We will accept and process a design regardless of its actual grid (as though it were completely design-rule legal) using the standard "recipe" for that design rule set.

The fracture process puts all its data onto a grid. As an example, the mask grid size in the case of the AMI 1.50 micron process is 0.05 micron on the critical layers (P1, P2 and Active) and 0.10 micron on the others, and all points in your layout that do not fall onto these grid points are "snapped" to the nearest grid point. Obviously, half a grid is the largest snap distance, applied to points that fall neatly in the middle.

---

8. XP Layer

MOSIS has defined an optional layer (called XP in CIF and numbered 26 in GDSII) to help users tell MOSIS which pads are to be bonded and which are not The bonding pad layer is named "XP" in all SCMOS technologies. This optional layer lets you call out only those glass cuts that you want MOSIS to use in bonding your project. This allows you to have probe pads within 600 micrometers (~25 mils) of the project edge, which MOSIS will not attempt to bond out.

Geometry on layer XP is used solely to help generate bonding diagrams. It has absolutely no influence on chip fabrication.

MOSIS XP and Pad Layer Checks:

MOSIS discovers the bonding pads in a project as follows:

A. If there is any layout on layer XP, MOSIS assumes that each rectangle on that layer -- either a box (B) or a polygon (P) -- that is at least 70 µm x 70 µm and within 600 micrometers of the project edge represents a bonding pad position.

B. If there is no layout on layer XP, MOSIS assumes that the distinct boxes (B) (but not polygons) of reasonable size and within 600 micrometers of the project edge - not overlapping and not touching - on the overglass cut layer represent bonding pad positions.

C. MOSIS checks that all declared bonding pads (in layer XP) have a glass cut feature under them. A project without these features will be rejected, and the user will receive the message: "Bonding marks (layer XP) without passivation cuts are not allowed."

D. MOSIS verifies that there is a metal pad under each bonding pad and will reject any project that does not have metal under glass cuts with the error message: "Bonding passivation cuts found without metal pads underneath.'

E. If you use the XP layer, MOSIS will not look at your glass cut layer to find your bonding pads. Therefore, be sure that the layout on this layer is correct, since the bonding diagram is generated based on these (presumed) bonding pads.

References

[1] C. Mead and L. Conway, *Introduction to VLSI Systems*, Addison-Wesley, 1980

[2] Cadence Design Systems, Inc./Calma. *GDSII Stream Format Manual*, Feb. 1987, Release 6.0, Documentation No. B97E060

[3] N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A System Perspective*, Addison-Wesley, 2nd edition, 1993